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EXAMINER	
TON, ANTHONY T	

ART UNIT	PAPER NUMBER
2661	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/643,566	TOMONAGA ET AL.	
	Examiner	Art Unit	
	Anthony T Ton	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *2,11-17 and 23-38* is/are allowed.

6)☒ Claim(s) *1,3,7-9 and 18-22* is/are rejected.

7)☒ Claim(s) *4-6 and 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 August 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTIONS

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

2. Claim **3** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 3 recites the limitation "the addresses" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 1, 3 and 7** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Larsson et al.** (US Patent No. **6,128,295**) in view of **Oba et al.** (US Patent No. **6,262,986**), hereafter referred to as **Larsson** and **Oba**, respectively.

a) **In Regarding to Claim 1**: **Larsson disclosed** a packet switch comprising:

an input buffer memory unit having a logic queue corresponding to an output line *(see Figs.1 and 2: buffer circuit and cell buffer; and Fig.15)*;

a control module for a first pointer indicating a scheduling start input line *(see Fig.2: 214; and Fig.15: 114 and 124)*;

a control module for a second pointer indicating a scheduling start output line of scheduling target outlines *(see Fig.2: 214; and Fig.15: 92 and 124)*;

a request management control module for retaining transmission request data about a desired output line *(see Fig.2: 110; and Figs.16A-16D and 17)*;

a packet buffer memory unit for temporarily storing a plurality of fixed-length packets and sequentially outputting the fixed-length packets *(see Fig.1: cell buffer; and Fig.3: 100)*;

a common switch unit for switching the fixed-length packets outputted from said packet buffer memory unit *(see Fig.1: 22)*; and

an address management unit for segmenting an address of said packet buffer memory unit into fixed-length blocks for a plurality of packets, and managing the address on a block basis *(see Fig.2 206)*.

Larsson failed to explicitly disclose a scheduling processing module for starting a retrieval from within plural pieces of transmission request data from the output line indicated by the second pointer, and selecting an output line that is not ensured by other input lines.

Oba disclosed such a scheduling processing module for starting a retrieval from within plural pieces of transmission request data from the output line indicated by the second pointer *(see Fig.2: 16)*.

At the time of the invention, it would be obvious to a person of ordinary skill in the art to combine such a scheduling processing module for starting a retrieval from within plural pieces of transmission request data from the output line indicated by the second pointer as taught by Oba

with Larsson, so that data packets can be properly routed through a packet switch. The motivation for doing so would have been to provide an order to read out packets stored in packet queues of a packet switch. Therefore, it would have been obvious to combine Oba and Larsson the invention as specified in this claim.

Both Larsson and Oba failed to disclosed the scheduling processing module for selecting an output line that is not ensured by other input lines. However, Larsson inherently disclosed such a scheduling processing module because Larsson disclosed a selector/scheduler in the buffer circuit 72 which selects a next appropriate physical link *(output line)* for switching data; wherein, an address of a cell buffer is placed in a free list for a second and last leaf of a cell for a physical link to be written to such a physical link *(see col.12 lines 16-53)*.

At the time of the invention, it would be obvious to a person of ordinary skill in the art to combine such a scheduling processing module for selecting an output line that is not ensured by other input lines teaching in the instant claim with Larsson, so that data information can be selected and routed to an output queue of a packet switch without any latency. The motivation for doing so would have been to provide an order to read out packets stored in packet queues of a packet switch. Therefore, it would have been obvious to combine the instant claim and Larsson the invention as specified in this claim.

b) **In Regarding to Claim 3**: **Larsson further disclosed** the packet switch according to claim 1, wherein said address management unit manages the addresses by flags indicating which sequence number in the block and which address related to this indicated sequence number a multicast is completed with *(see col.3 lines 13-35)*.

c) **In Regarding to Claim 7**: **Larsson disclosed** all aspects of this claim as set forth in claim 1, and **Larsson further disclosed** wherein said packet buffer memory executes time-division-multiplexing of the fixed-length packets of the plurality of input lines onto one signal input line in an established manner *(see col.1 lines 24-36)*.

Larsson failed to explicitly disclosed wherein said packet buffer memory includes memories disposed in parallel corresponding to every input line before being multiplexed, and the writing and reading to and from said respective memories are executed in parallel.

Oba disclosed such a packet buffer memory includes memories disposed in parallel corresponding to every input line before being multiplexed, and the writing and reading to and from said respective memories are executed in parallel *(see Fig.10)*.

At the time of the invention, it would be obvious to a person of ordinary skill in the art to combine such a packet buffer memory includes memories disposed in parallel corresponding to every input line before being multiplexed, and the writing and reading to and from said respective memories are executed in parallel as taught by Oba with Larsson, so that data packets in each input queue can be properly routed to a corresponding output queue. The motivation for doing so would have been to provide an order to read out packets stored in input packet queues of a packet switch and reduce delay variation on other processes. Therefore, it would have been obvious to combine Oba and Larsson the invention as specified in this claim.

5. **Claims 8 and 9** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Larsson** (US Patent No. **6,128,295**) in view of **Caldara et al.** (US Patent No. **6,141,346**), hereafter referred to as **Caldara**.

a) **In Regarding to Claim 8**: **Larsson disclosed** all aspects of this claim as set forth in claim 1.

Larsson failed to explicitly disclosed packet switch according to claim 1, wherein said common switch unit is based on a bit-slice architecture and has slice switches of which at least one slice switch is used as a redundant switch, and switching to said redundant slice switch can be thereby done every time said slice switch receives maintenance and comes to a fault.

Caldara disclosed such a common switch unit is based on a bit-slice architecture and has slice switches of which at least one slice switch is used as a redundant switch, and switching to said redundant slice switch can be thereby done every time said slice switch receives maintenance and comes to a fault *(see Fig.1 and claim 1)*.

At the time of the invention, it would be obvious to a person of ordinary skill in the art to combine such a common switch unit is based on a bit-slice architecture and has slice switches of which at least one slice switch is used as a redundant switch, and switching to said redundant slice switch can be thereby done every time said slice switch receives maintenance and comes to a fault, as taught by Caldara with Larsson, so that data packets in each input queue can be reached to a corresponding output queue in different paths. The motivation for doing so would have been to provide a backup path for preventing data loss. Therefore, it would have been obvious to combine Caldara and Larsson the invention as specified in this claim.

b) **In Regarding to Claim 9**: the claimed subject matters of this claim are similar to that of the claim 8. Therefore, the rejection to the claim 8 would apply to the rejection of this claim as **a packet buffer memory unit** as taught by the instant claim.

6. **Claims 18 and 19** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Oba** (US Patent No. **6,262,986**) in view of **Steely, Jr. et al.** (US Patent No. **6,249,520**), hereinafter referred to as Steely.

a) **In Regarding to Claim 18**: **Oba disclosed** a packet switch comprising:

a scheduling processing module for executing a scheduling process at a certain fixed speed *(see Fig.2 and col.1 lines 19-10: CBR)*;

a first timer processing module for measuring a packet slot time obtained from a scheduling speed for an input line speed *(see Fig.3: 36; and col.11 lines 23-52: TDM like scheduling with respect to the classes; and cell number counter for class c if s=1 for input, the state register 36 in Fig.3 is considered as a first timer processing module)*; and

a second timer processing module for measuring a packet slot time obtained from a scheduling speed for an output line speed *(see Fig.3: 36; and col.11 lines 23-52: TDM like scheduling with respect to the classes; and cell number counter for class c if s=2 for output, hence the state register 36 in Fig.3 is also considered as a second timer processing module)*, and

wherein when the scheduling process for a certain input line is executed *(see Fig.7)*, said first timer processing module starts the measurement *(see Fig.7 step S220, set state register value of the state register 36 as shown in Fig.6 = 0)*.

Oba failed to explicitly disclosed the scheduling process for that input line is stopped during a period for which said first timer processing module thereafter measures a predetermined time, and the scheduling process corresponding to the input line speed is thus actualized.

Steely disclosed such a scheduling process *(see Fig.2, Figs.12A-12B and Fig.13; and Figs.21 and 22: T8 No Write Executed)*.

At the time of the invention, it would be obvious to a person of ordinary skill in the art to combine such a scheduling process, as taught by Steely with Oba, so that data packets in each input queue can be controlled and transmitted to a corresponding output queue properly. The motivation for doing so would have been to provide overflow controls in data packet switching network. Therefore, it would have been obvious to combine Steely and Oba the invention as specified in this claim.

b) **In Regarding to Claim 19**: **Oba disclosed** all aspects of this claim as set forth in claim 18, and Oba further disclosed wherein when an establishment for a certain output line is made, said second timer processing module starts the measurement *(see Fig.7 when s=2 and step S220, set state register value of the state register 36 as shown in Fig.6 = 0).*

Oba failed to explicitly disclosed an establishment for the same output line is stopped during a period for which said second timer processing module thereafter measures a predetermined time, and a traffic flow to the same output line is restrained to an output line speed or lower. However, this subject matter is similar to that as set forth in claim 18 for the input line.

At the time of the invention, it would be obvious to a person of ordinary skill in the art to combine such an establishment, as taught by Steely with Oba, so that data packets in each output queue can be controlled properly. The motivation for doing so would have been to provide overflow controls in data packet switching network. Therefore, it would have been obvious to combine Steely and Oba the invention as specified in this claim.

7. **Claim 20** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Oba** (US Patent No. **6,262,986**) in view of **Linville et al.** (US Patent No. **6,026,075**), hereinafter referred to as Linville.

Oba disclosed all aspects of this claim as set forth in claim 18.

Oba failed to explicitly disclosed the packet switch according to claim 18, wherein the start of the measurement of each of said first and second timer processing modules is triggered neither by scheduling nor by the establishment but by a fixed time interval.

Linville disclosed such a fixed time interval trigger *(see col.8 lines 51-61)*.

At the time of the invention, it would be obvious to a person of ordinary skill in the art to combine such a fixed time interval trigger, as taught by Linville with Oba, so that a physical link in a packet switch in a communication network can be active other time. The motivation for doing so would have been to avoid shutting down a link in a packet switch network. Therefore, it would have been obvious to combine Linville and Oba the invention as specified in this claim.

8. **Claims 21 and 22 are** rejected under 35 U.S.C. 103(a) as being unpatentable over **Oba** (US Patent No. **6,262,986**) in view of **Ha-Duong et al.** (US Patent No. **6,181,678**), hereinafter referred to as Ha-Duong.

a) **In Regarding to Claim 22**: **Oba disclosed** all aspects of these claims as set forth in claim 18.

Oba failed to explicitly disclosed wherein when the scheduling process is executed in a way of pipeline processing, the scheduling for a relevant input line at pipeline processing N-stages anterior and posterior on the basis of a ratio of a scheduling speed to an input line

speed, is stopped, and the scheduling corresponding to the input line speed is thereby actualized; and

Ha-Duong disclosed such a pipeline processing *(see abstract, Fig.2: registers 0-3, Fig.5; and col.2 line 58-col.3 line 15).*

At the time of the invention, it would be obvious to a person of ordinary skill in the art to combine such a pipeline processing, as taught by Ha-Duong with Oba, so that the controllers of pipelines can be operated in parallel. The motivation for doing so would have been to provide time efficiency. Therefore, it would have been obvious to combine Ha-Duong and Oba the invention as specified in this claim.

b) **In Regarding to Claim 22**: the claimed subject matters of this claim are similar to that of the claim 21. Therefore, the rejection to the claim 21 would apply to the rejection of this claim as wherein said **second timer processing module**, when executing the scheduling process in a way of pipeline processing, executes the control independently for every pipeline process on the basis of a pipeline number and an output line number as taught by the instant claim.

Allowable Subject Matter

9. **Claims 2, 11-17 and 23-38** are allowed.

10. **Claims 4-6 and 10** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Remarks

11. Applicant's Remarks filed on 04/13/2004 with respect to claims 1-38 have been considered but are moot in view of the new ground(s) of rejection.

Examiner Information

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anthony T. Ton whose telephone number is 703-305-8956. The examiner can normally be reached on Monday-Friday from 8:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Douglas W Olms, can be reached on (703) 305-4703. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

ATT
6/24/2004

Phirin Sam